



BUK7Y20-30B

N-channel TrenchMOS standard level FET

Rev. 04 — 7 April 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using Nexperia High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V Loads
- Automotive systems
- General purpose power switch
- Motors, lamps and solenoids

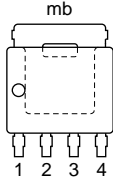
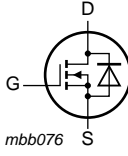
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25 \text{ °C}$; $T_j \leq 175 \text{ °C}$	-	-	30	V
I_D	drain current	$V_{GS} = 10 \text{ V}$; $T_{mb} = 25 \text{ °C}$; see Figure 1 ; see Figure 4	-	-	39.5	A
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ °C}$; see Figure 2	-	-	59	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 20 \text{ A}$; $T_j = 25 \text{ °C}$; see Figure 12 ; see Figure 13	-	16	20	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 39.5 \text{ A}$; $V_{sup} \leq 30 \text{ V}$; $R_{GS} = 50 \text{ Ω}$; $V_{GS} = 10 \text{ V}$; $T_{j(init)} = 25 \text{ °C}$; unclamped	-	-	45	mJ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 20 \text{ A}$; $V_{DS} = 24 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 14	-	3.84	-	nC

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LFPAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7Y20-30B	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	-	30	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 ; see Figure 4	-	-	39.5	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	-	28	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 4	-	-	158	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	59	W
T_{stg}	storage temperature		-55	-	175	°C
T_j	junction temperature		-55	-	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	-	-	39.5	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ °C}$	-	-	158	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 39.5\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	-	-	45	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[1] [2] [3]	-	-	J

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[2] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

[3] Refer to application note AN10273 for further information.

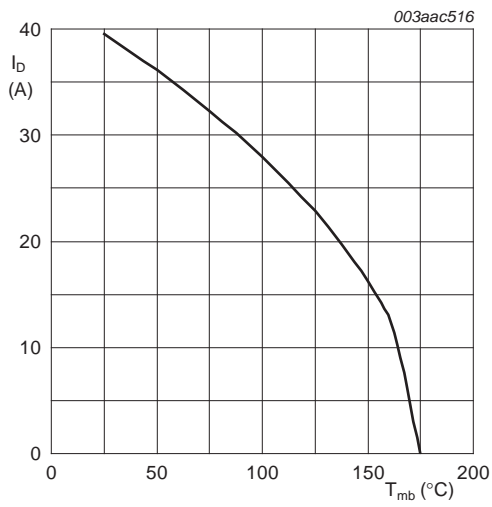
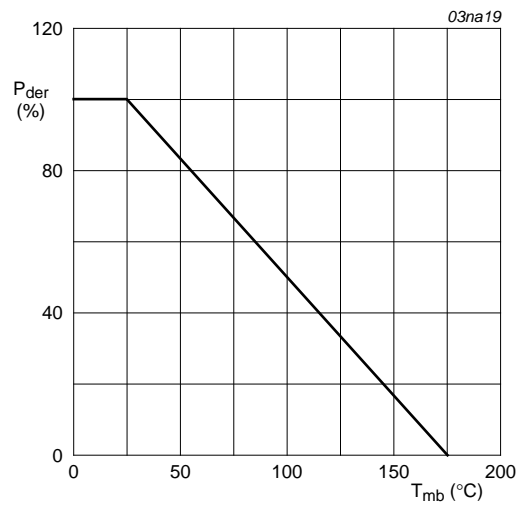


Fig. 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig. 2. Normalized total power dissipation as a function of mounting base temperature

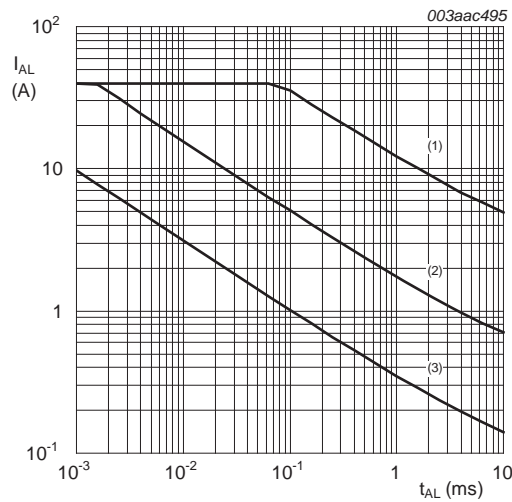
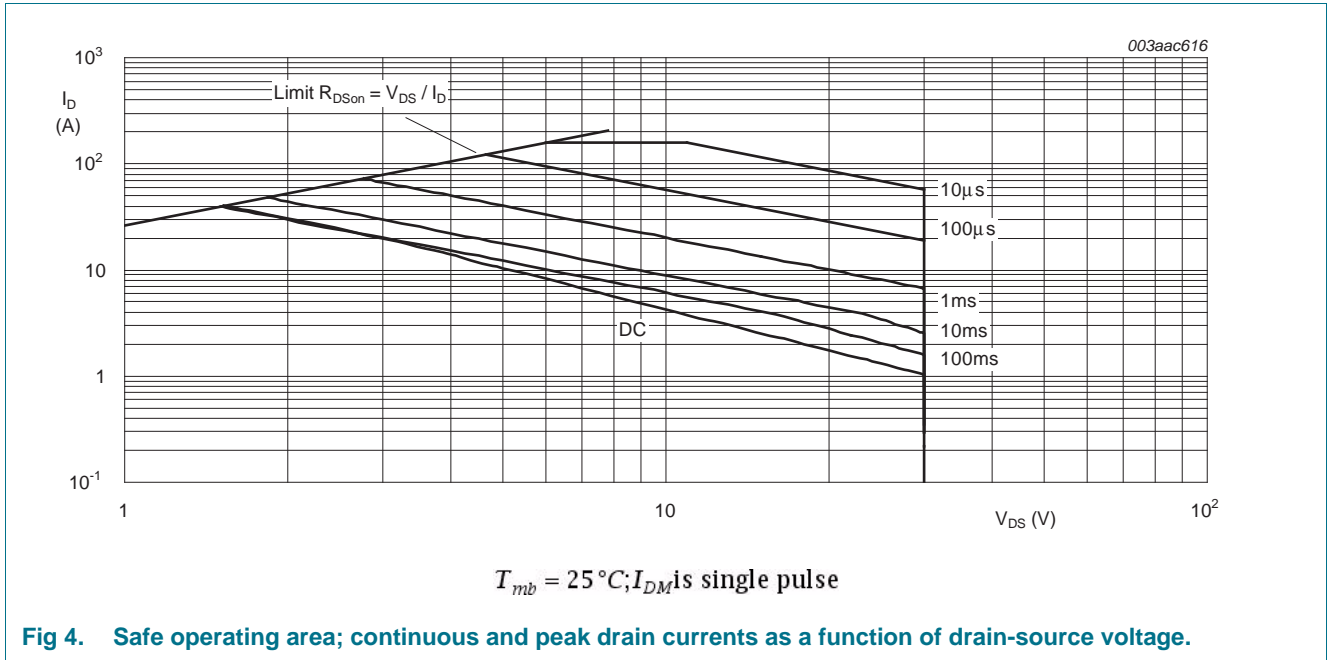


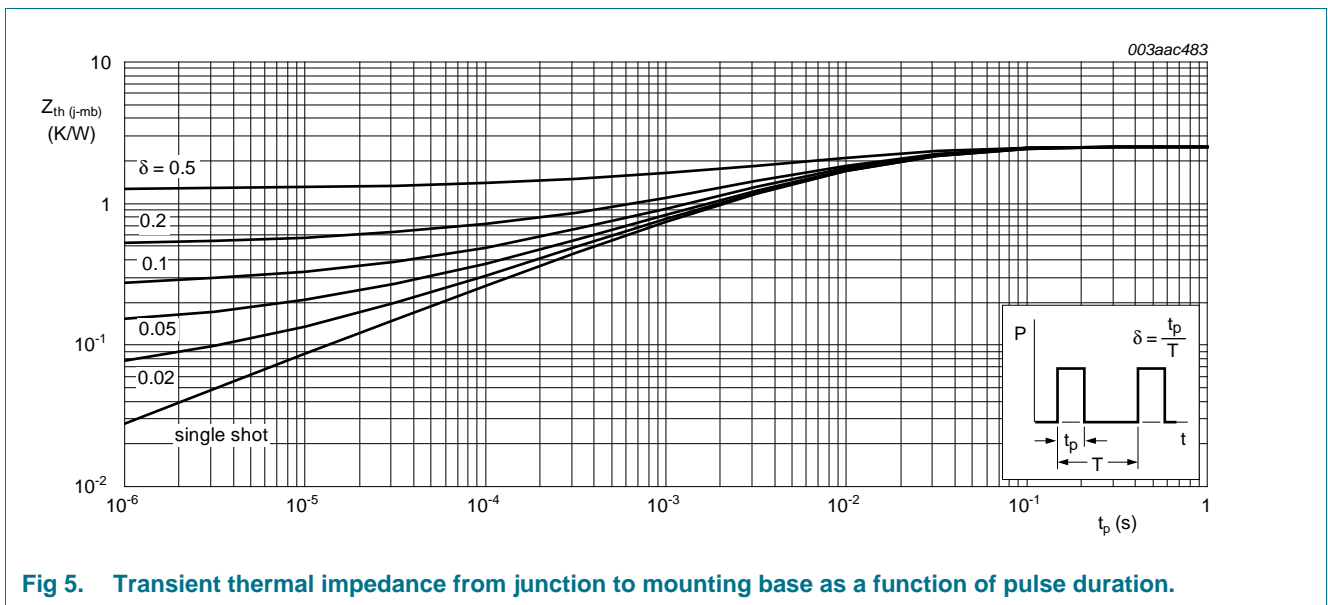
Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



5. Thermal characteristics

Table 5. Thermal characteristics

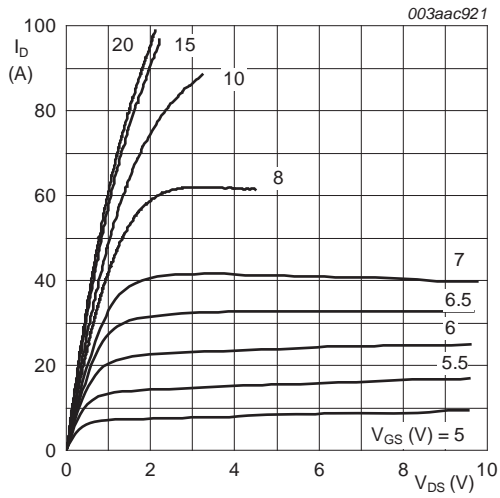
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	2.53	K/W



6. Characteristics

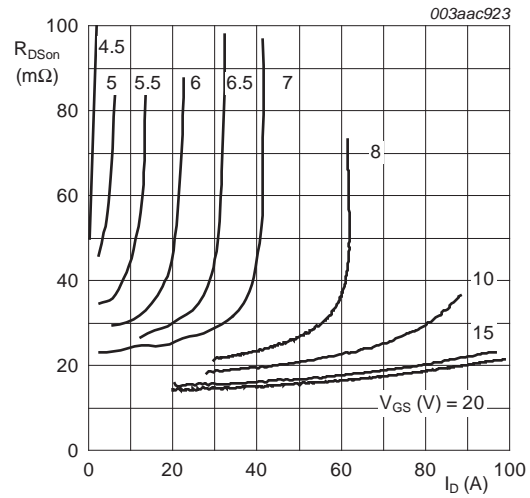
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10	-	-	4.4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 10	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see Figure 12	-	-	38	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 12 ; see Figure 13	-	16	20	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 20 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 14	-	11.2	-	nC
Q_{GS}	gate-source charge		-	3.75	-	nC
Q_{GD}	gate-drain charge		-	3.84	-	nC
C_{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 15	-	516	688	pF
C_{oss}	output capacitance		-	188	226	pF
C_{rss}	reverse transfer capacitance		-	94	129	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 25 \text{ V}; R_L = 1.25 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega$	-	9.5	-	ns
t_r	rise time		-	18	-	ns
$t_{d(off)}$	turn-off delay time		-	20.5	-	ns
t_f	fall time		-	10	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 25 \text{ V}$	-	28	-	ns
Q_r	recovered charge		-	27.4	-	nC



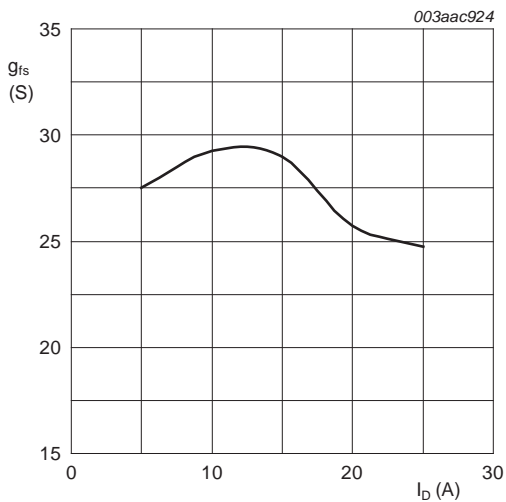
$T_j = 25^\circ\text{C}$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.



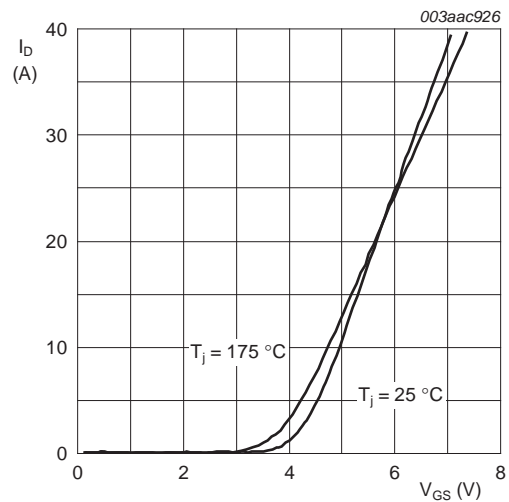
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



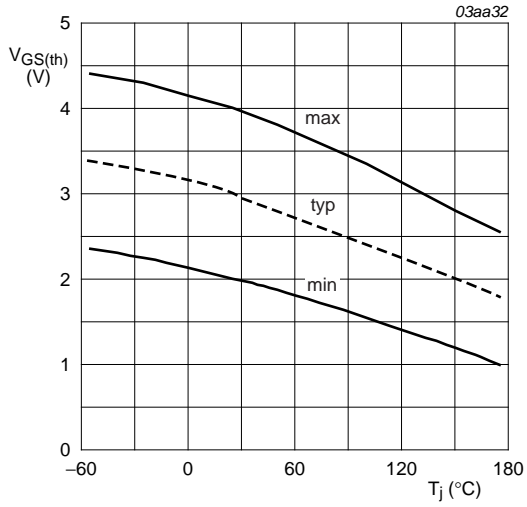
$T_j = 25^\circ\text{C}; V_{DS} = 25\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values.



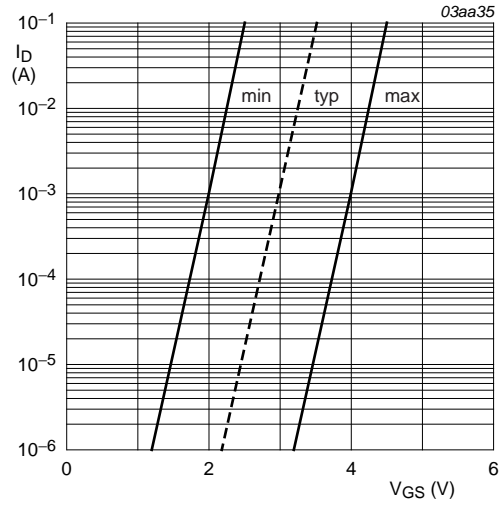
$V_{DS} = 25\text{V}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



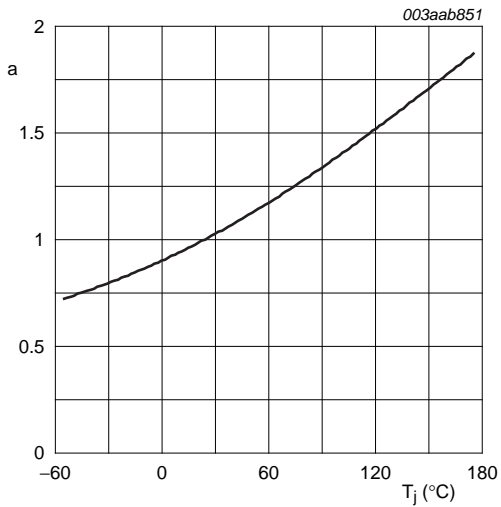
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



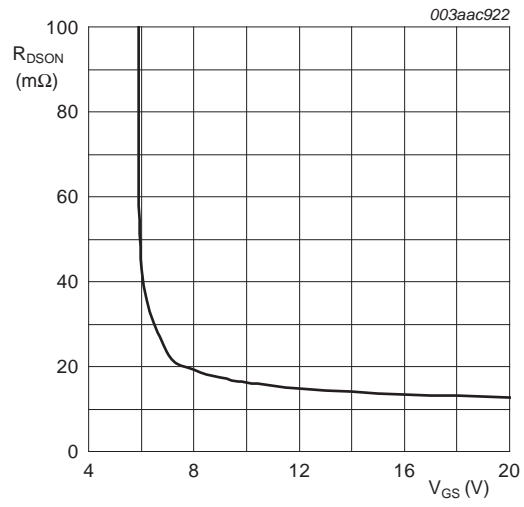
$$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{V}$$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



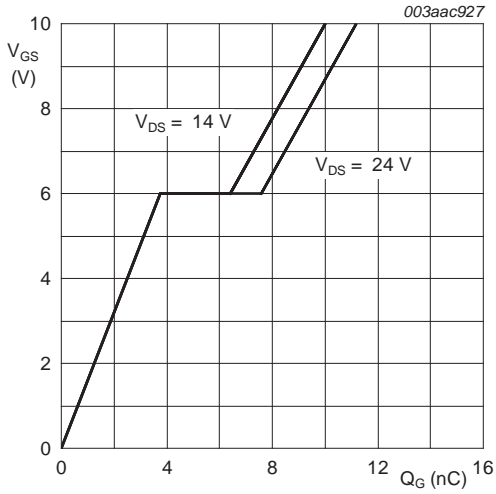
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



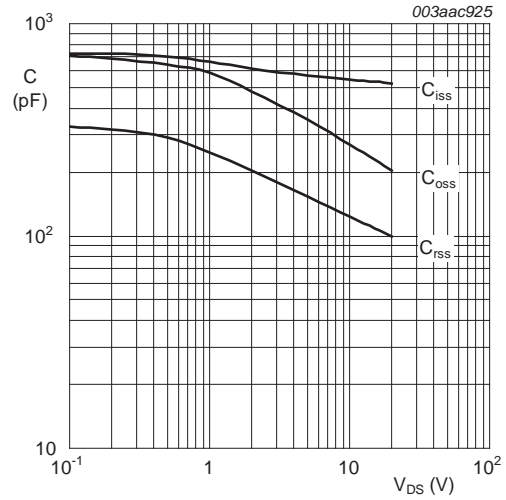
$$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{A}$$

Fig 13. Drain-source on-state resistance as a function of gate-source voltage; typical values.



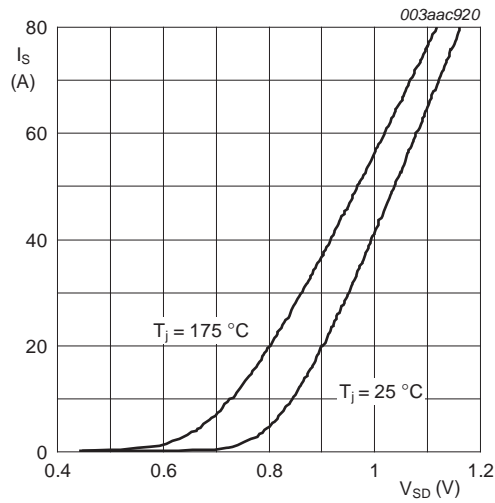
$T_j = 25\text{ }^\circ\text{C}; I_D = 20\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values.



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



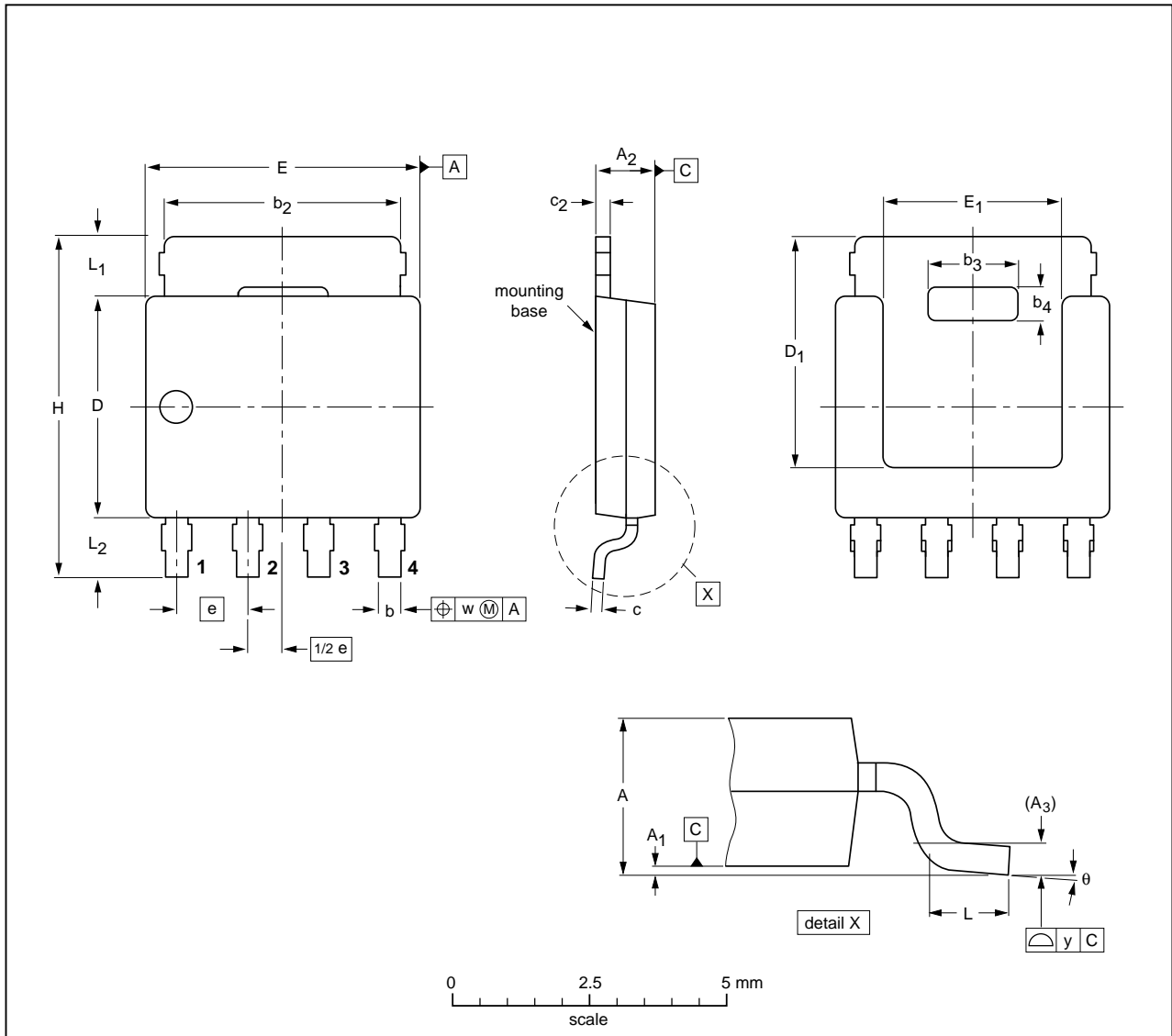
$V_{GS} \geq 0\text{ V}$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾ _{max}	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				04-10-13 06-03-16

Fig 17. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7Y20-30B_4	20100407	Product data sheet	-	BUK7Y20-30B_3
Modifications:	• Status changed from objective to product			
BUK7Y20-30B_3	20100217	Objective data sheet	-	BUK7Y20-30B_2

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	3
5	Thermal characteristics	5
6	Characteristics	6
7	Package outline	10
8	Revision history	11
9	Legal information	12
9.1	Data sheet status	12
9.2	Definitions	12
9.3	Disclaimers	12
9.4	Trademarks	13
10	Contact information	13